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EXAMINER
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ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/188,241	LUO, WENZHE	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2002 and 09 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,18,19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,18,19,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *04 November 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment/Drawings/RCE

The amendment and drawing correction submitted on Nov 4, 2002, and the RCE submitted on Dec 9, 2002, have been reviewed and considered with the following results:

The RCE was approved and entered. Therefore, the amendment and drawing correction were also entered.

The proposed drawing correction for Fig 2 has been approved. Therefore, that objection has been withdrawn.

The objection to the specification has been modified, and is described later. As the examiner has previously pointed out to the applicant, the description on page 7 is considered inconsistent and confusing. Consistent labeling within the disclosure would help to clarify what the applicant is trying to convey. However, it appears the applicant is content on submitting comments that not only do not clarify the confusion, but actually adds to it. See the Response to Arguments section for more details.

The prior art rejections have been maintained, with some variations related to the amended changes within the claims. These rejections are described later under the appropriate section, and associated comments are described under the Response to Arguments section.

Specification

The disclosure remains objected to because of the following informalities: The description on page 7, lines 17-22 is confusing. As long as current is flowing through

MC, its load side (i.e. lower side of MC) current and current source side (i.e. upper side of MC) current are considered the same/equal. As such, how can amplifier 400 equalize a current level that is already equal? It is believed that any change of current at either the current source side or the load side of MC will directly affect the current at the other side. If switch MS is turned off (e.g. see lines 20-22), there will be no current path for charge injection from the current source MC to load capacitor CL. Therefore, clarification is still required in order to determine what the applicant is actually trying to convey. Also related to lines 18-21 of page 7, it is not understood why the labeling of "MC" is inconsistent. For example, lines 1-2 and 29 relate MC with a "current source", but lines 18 and 19 both refer to it as a "switch." Only with at least one of switches MT or MS would the examiner consider MC a switched current source, because once a power supply and VBIAS are applied to MC, it is believed MC will continuously conduct current (through a respective path related to MT and MS). Therefore, why would MC itself be considered a "switch" since it remains on? Appropriate corrections and/or clarifications are required which will help the examiner determine what the applicant is attempting to describe.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14, 18, 19, 21 and 22 remain rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. After reading the

applicant's comments, it is no longer clear what the applicant considers the load as recited within the independent claims (e.g. see claim 1, lines 7 and 10; claim 18, lines 2 and 11; claim 21, line 1, 4, 10 and 12; and claim 22, lines 1, 4, 11 and 13). For example, page 7 of the amendment clearly indicates that all the components connected to the drain of current switch/transistor MC (e.g. shown in the applicant's Fig. 5) act as a load. Therefore, it appears the applicant considers switch 430, pull-down mirror path 450, and load capacitor 440 as MC's load. Therefore, clarification is requested with respect to what constitutes the "load" recited within the claimed invention(s). It is still not clear in independent claims 1 (line 6), 18 (lines 4-5), 21 (lines 8-9), and 22 (lines 9-10) what "to equalize a current level produced by said current source" means. For example, if the currents on both sides of a current source are (substantially) equal, it would be obvious to one of ordinary skill in the art that a MOS transistor used as a current source will have equal currents at its source and drain. Also, if the current source is providing a predetermined, constant current, that current could be considered equal to its desired operational current. Since the applicant's own figures do not show how current would actually flow in the pull-down path, it is not clear how the current of the applicant's own current source is equalized. Using the applicant's own Fig. 5 as an example, it is assumed that current flowing into pull-down mirror path 450 (when switch MT is closed) will be equal to the current flowing through switch MS when it is closed. However, since there are only two current paths for current IA from current source MC to flow into, and only one path is on at any one time, it would be obvious to one of ordinary skill in the art that those current paths would contain an equal amount of current with respect to when

the current flows within the paths. On the other hand, since one current path is always opened when the other path is closed, the current flow within the closed path will be much greater than the current flow (e.g. possibly due to some leakage) within the opened path, and their respective current levels will not be equalized. Therefore, clarification is still requested with respect to what the applicant considers "operating to equalize a current level produced by said current source." The description "substantially continuously receives said current flowing from said current source" in claims 21 (lines 10-11) and 22 (lines 11-12) is still considered misleading. For example, if only 440 is considered the load within the applicant's Fig. 5, current IA from current source 420 will flow to load 440 only when transistor switch 430 is conducting. However, when transistor switch 430 is open, current IA cannot flow from the current source to the load. Therefore, how can the switch/pull-down mirror path "substantially continuously" reduce charge injection when switch 430 is open? Since current IA would be flowing through (or into) the pull-down mirror path when switch 430 is open, no current or charge injection would be "flowing to" the load from current source 420. Also, as long as switch 430 is closed, the load will always receive the current flow from the current source unless the load is allowed to become fully charged, and at that time, current flow would then cease. Therefore, as long as switch 430 is closed, there will be no charge injection related to switch 430 because of the lack of switching operations. If the pull-down mirror path and transistor switch are considered part of the load (as implied by the amendment's page 7 description), then the transistor switch of claims 21 and 22 would not be considered as actually connecting the current source to the load. For example, if

430-450 of the applicant's Fig. 5 are considered the load, then current source 420 is always connected to the load. Also, as long as current flows through current source 420, it will be flowing into one of two paths within load 430-450. If only 440 is considered the load, it cannot continuously receive a current flow from current source 420 because once switch 430 is opened, the current path between current source 420 and load 440 is broken as previously described. Therefore, clarification is requested with respect to what the applicant actually considers the load, and what is meant by "continuously receives said current flowing from said current source" as recited within the claims. The use of "during switching of said current source while said current source remains powered" within claims 1 (lines 10-11), 18 (lines 12-13), 21 (lines 12-13), and 22 (lines 13-14) is considered misleading. When considering the applicant's own Fig. 5, as long as current source 420 remains powered, it is believed it will continuously provide current IA. Therefore, the current source itself is not switched. However, its current is selectively switched through a current path (i.e. 450 or 430,440) by respective switches MT (within 450) and MS (within 430,440).

Dependent claims carry over the rejection from their respective independent claim.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 1-5, 8-10, 12, 18, 19, 21, and 22 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon, a reference cited in previous Office Actions. For the following descriptions, Figs. 2-4 of Ravon will be considered and/or referred to, wherein one of ordinary skill in the art would be able to recognize the relationships between the figures. In Fig. 2, Ravon shows a current source switching circuit comprising a current source 11; transistor switch M1; what can be deemed a pull-down mirror path M2,13,14 in parallel with transistor switch M1 (e.g. they are both coupled between terminal E and ground); and first load C',2. Current source 11 is shown in detail in Fig. 3 (see column 4, lines 44-45), and is disclosed as providing a constant current I (e.g. see column 3, line 31 and column 4, lines 44-45). Fig. 4 shows part C' of first load C',2, transistor M2, and details of comparator 14. Although transistor switch M1 is replaced by diode D1 in Fig. 4 (see column 6, lines 16-18), Ravon also discloses a transistor provides better efficiency on column 6, lines 24-25. Therefore, for the following description, diode D1 of Fig. 4 will be replaced with a transistor switch (e.g. M1 of Fig. 2) for improved efficiency, wherein block 13 of Fig. 2 will be used to control the on/off operations of both transistors M1 and M2. One of ordinary skill in the art would recognize that current source 11 (shown in Figs. 2 and 3) provides current I to terminal E of Fig. 4. Although the reference does not clearly

disclose the "substantially continuously" reduction of "charge injection" as recited within the claims, one of ordinary skill in the art would know it relates to the current received by the load C',2 from the current source when transistors M2 and M1 are switched off and on. For example, when transistor M2 is switched off and transistor switch M1 is switched on, first load C',2 receives current I (from current source 11) through transistor switch M1 (e.g. see Fig. 2). Besides charging first load part C', the current also charges capacitor C1 through resistor R1 (see Fig. 4). [Note that the structure of first load C',2, capacitor C1, resistor R1, and amplifier 20 closely corresponds to the respective load 440, capacitor C1, resistor R1, and amplifier 400 structure of the applicant's Fig. 5.] As long as current source 11 remains powered, when transistor switch M1 is switched off, and transistor M2 is switched on, capacitor C1 will help maintain the voltage across first load C',2 (i.e. between terminal S and ground). Therefore, less current will be required to completely charge first load C',2 back up once transistor switch M1 is switched back on. Also, since current I is constant, the current flowing through M2 will be equal to the current flowing through M1, when the respective transistor is conducting (i.e. switched on). After switching switch M1 on and M2 off, transistor switch M1 and pull-down mirror path M2,13,14 will substantially continuously reduce the charge injection into first load C',2. For example, when switch M1 is switched off and switch M2 is switched on, current I does not flow to load C',2, but flows through switch M2. Therefore, there will be no current I flow into load C'.2 from current source 11, and charge injection "flowing to" the load is reduced. As long as current source 11 remains powered, when switch M1 is switched on and switch M2 is switched off, current I will flow to load C',2, until the

load is fully charged, or until M1 and M2 are switched into their off and on states, respectively. Therefore, during the periods when switches M1 and M2 are held in the on and the off states, respectively, charge injection is considered to be substantially continuously reduced with respect to the flow to load C',2, rendering claim 1 obvious. [The voltage at terminal S will be basically maintained across first load C',2 by the voltage held across capacitor C1, when switch M1 is not conducting. Therefore, once switch M1 is switched on, current I will flow through switch M1 and into load C',2 without any abrupt changes of voltage and current, thus reducing charge injection related to the switching operation.] Fig. 2 clearly shows current source 11 connected between power source Vc and a first side (i.e. terminal E) of transistor switch M1, and first load C',2 connected between ground and a second side (i.e. terminal S) of transistor switch M1, thus claims 2 and 3 are rendered obvious. Since first load C',2 has a charging capacitor C', and transistor M1 is a MOS transistor, claims 4 and 5 are rendered obvious. Transistor M2 of the pull-down mirror path M2,13,14 can be deemed a pull-down amplifier (e.g. transistors can be deemed one type of an amplifier), rendering claim 8 obvious. When transistor M2 is conducting, its output (i.e. drain) follows the current source 11 side of the transistor switch M1 by allowing the current to flow through transistor M2, thus claim 9 is also rendered obvious. Transistors M1 and M2 receive their respective signals from control 13 (see Fig. 2) which allows transistor M2 to be turned off, and then transistor M1 to be turned on (see column 4, lines 28-30). Therefore, transistor M2 is deemed a complementary type pull-down mirror path transistor switch, which operates opposite the transistor switch M1 (e.g. one is typically

on while the other is off), rendering obvious claim 10. Since current source 11 comprises MOS transistor M3 (e.g. see Fig. 3), claim 12 is rendered obvious. Transistor/switch M2 provides a pull-down mirror path parallel with current switch M1 (e.g. coupled between terminal E and ground), wherein switches M2 and M1 are substantially turned on and off alternatively, rendering obvious claims 18 and 19 because when transistor M1 is off, the capacitor C1 will basically maintain a voltage on load capacitor C', thus substantially continuously reducing the charge injection flowing to the load (e.g. no current) while equalizing the current flow (e.g. current I will flow through either M1 or M2, depending on which one is conducting) as previously explained above. Transistor switch M1 connects current source 11 to load C',2, and it is substantially simultaneously turned off when switch M2 is turned on. When switch M2 is on, the current I from current source 11 flows through the pull-down mirror path M2,13, 14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C',2, the charge injection will be reduced when transistor switch M1 is switched off, rendering obvious claim 21. The upper output of block 13 is coupled to the gate of transistor switch M1 and is deemed the means for switching open transistor switch M1, and the lower output of block 13 is coupled to the gate of switch M2 and is deemed the means for switching close switch M2, wherein current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C',2, the charge injection is considered to be substantially continuously reduced when transistor switch M1 is switched opened, rendering claim 22 obvious.

Claims 6, 7 and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to respective claims 1 and 10 above, and further in view of the applicant's Prior Art Fig. 3. As described previously, the basic current source switching circuit is shown and disclosed by the reference of Ravon. However, the reference does not show or disclose the use of the serial combinations of transistors as recited within claims 6, 7 and 11. Ravon shows only a single transistor for transistor switch M1 and one transistor for complementary pull-down mirror path transistor switch M2. It would have been obvious to one of ordinary skill in the art to replace each of transistors M1 and M2 of Ravon's circuit with a respective compensated transistor switch of the applicant's Prior Art Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/ well known means for reducing charge injection. Since Ravon's circuit can be considered a current type switch circuit for charging first load C',2, the compensated switch of the applicant's Fig. 3 would help reduce charge injection even more within the circuit if that was desired.

Claims 13 and 14 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to claim 1 above. As described previously, Figs. 2 and 4 of

Ravon show a circuit with a transistor switch M1, pull-down mirror path M2,13,14, current source 11, and first load C',2. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuitry of Ravon by reversing the polarities (i.e. Vc and ground would be reversed) and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage (e.g. closer to power source Vc). The reversal would replace all the MOS transistors (i.e. M1-M6) with their complementary transistors (i.e. an NMOS transistor would be replaced with a PMOS transistor). In this case, transistor M2 would be coupled between power source Vc and the common connection of current source 11/transistor switch M1, and first load C',2 would be coupled between power source Vc and terminal S. Therefore, transistor M2 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 11 would be coupled between ground and one side (i.e. terminal E) of transistor switch M1, rendering obvious claim 14.

In so far as being understood, claims 1-5, 8-10, 12, 18 and 19 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston, another reference cited in previous Office Actions. In Fig. 3 Harston shows a current source switching circuit comprising current source MP1; transistor switch MP2; a pull-down mirror path MP3 in parallel with transistor switch MP2; and first load 10pf. Although the reference does not clearly disclose a substantially continuously reduction in charge injection, it would be obvious to one of ordinary skill in the art that resistor 37.5Ω, and the switching operations of MP2 and MP3, would substantially continuously reduce the charge

injection flowing to first load 10pf. For example, when transistor switch MP2 is off, the current from current source MP1 will flow through MP3 to ground. Since the current that flows through MP2 and MP3 is from the same current source, they are deemed equalized. Also, when current is flowing through MP3 (and not MP2), and there is still a charge on first load 10pf, the current flowing to the first load will be reduced because the load will be disconnected from the current source, and current will actually flow from the load through the resistor. After transistor switch MP2 is initially switched back on, there will be a substantially continuously reduction of charge injection flowing to load 10pf because when there is no switching, there is no charge injection occurring (with respect to the switching operation), and current will flow from current source MP1 to load 10pf. Therefore, claim 1 is rendered obvious. [MP3 is considered a pull-down mirror path since it mirrors the operation of the transistor switch MP2 and allows the current from transistor MP1 to flow down to ground when switch MP2 is not conducting. See column 2, lines 64-68.] Fig. 3 also shows a current source MP1 (a MOS transistor) coupled between power source CURRENT CELL and the first side of transistor switch MP2; and load 10pf is a charging capacitor 10pf coupled between ground and a second side of transistor switch MP2, thus rendering obvious claims 2-5. Since a transistor can be deemed an amplifier, pull-down mirror path MP3 can be deemed a pull-down amplifier, rendering claim 8 obvious. When transistor MP3 is conducting, its output (i.e. drain) follows the current source MP1 side of the transistor switch MP2 by allowing the current to flow through transistor MP3, thus rendering obvious claim 9. Transistors MP2 and MP3 receive their respective signals DATAB and DATA. Therefore, transistor MP3 can

be deemed a complementary pull-down mirror path transistor switch operating the opposite of transistor switch MP2, rendering claim 10 obvious. It is complementary since it receives a control signal which is a complement of the signal received by transistor switch MP2. Since current source MP1 is a MOS transistor, claim 12 is rendered obvious. Transistor/switch MP3 provides a pull-down mirror path parallel with current switch MP2, wherein switches MP3 and MP2 are alternatively on and off, rendering obvious claims 18 and 19 because when transistor MP2 is off, the resistor 37.5Ω will discharge load 10pf, thus substantially continuously reducing the charge injection flowing to the load as previously described. For example, when the load capacitor is discharging, the current will flow away from the load. Therefore, there will be no charge injection flowing to the load, and the charge injection will be substantially continuously reduced as long as MP2 is not conducting. Also, when MP2 begins conducting before load capacitor 10pf has completely discharged through resistor 37.5Ω, the current (e.g. charge injection) required to charge the load capacitor back up will be less, and as long as switch MP2 is on, the charge injection will be reduced. Therefore, it would be obvious to one of ordinary skill in the art that the charge injection flowing to the load, under the conditions described above, can still be considered substantially continuously reduced.

Claims 6, 7, and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to their respective claim 1 or 10 described above, and further in view of the compensated transistor switch of the applicant's Prior Art Fig. 3. Harston shows only a single transistor for each of transistor switch MP2 and

complementary pull-down mirror path transistor switch MP3. It would have been obvious to one of ordinary skill in the art to replace each of the single transistors MP2 and MP3 of Harston's circuit with a respective compensated transistor switch of the applicant's Prior Art Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection of switches in analog circuits. Since Harston's circuit in Fig. 3 can be considered a current switch circuit related to an analog circuit, the compensated switch of Fig. 3 would help reduce charge injection within the circuit if that was desired.

Claims 13 and 14 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to claim 1 above. As described previously, Fig. 3 of Harston shows a circuit with a transistor switch MP2 (30), pull-down mirror path MP3 (32), current source MP1 (20), and load capacitor 10pf. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuit of Fig. 3 by reversing the polarities and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage. The reversal would replace all the PMOS transistors (i.e. MP1, MP2 and MP3) with NMOS transistors. In this case

transistor 32 would be coupled between power source CURRENT CELL and the common connection of current source 20 and transistor switch 30. Therefore, transistor 32 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 20 would be coupled between ground and one side of transistor switch 30, rendering obvious claim 14.

No claim is allowable. Claims 15-17, and 20 had been canceled previously.

Response to Arguments

The applicant's arguments filed Nov 4, 2002 have been fully considered but they are not persuasive. The applicant argues: 1) the finality of the previous Office Action was improper; 2) the labeling of the switches on page 7 are correct; 3) all other components (connected to the drain leg of transistor MC) act as a load); 4) the current level of the current source is equalized with respect to itself; 5) the load substantially continuously receives current from the current source; 6) the mirror path diverts the charge injection to ground; 7) applicant repeatedly tries to convey the charge injection is associated with a switched current source (i.e. 420), not switch 430; 8) with respect to the Ravon reference, the load creates the current fluctuations, the examiner rejected the claims as being anticipated, and Ravon does not teach the reduction of charge rejection; 9) Hartson fails to disclose, teach, or suggest the reduction of charge rejection; and 10) the switch MC is NOT biased by a reference voltage.

1) Page 6 of the amendment indicates the finality of the previous Office Action was improper because of "**numerous** new grounds." However, it is believed the applicant did not take into account the modified rejections by the examiner were made

with respect to changes the applicant had made in the amended claims. Therefore, those "numerous new grounds" were in response to the applicant's own changes and comments.

2) Although the applicant's comments on pages 6-7 of the amendment indicate the labeling of the switches on page 7 are correct, the examiner still disagrees. For example, why is "MC" identified as a "switch" on lines 18 and 19, and then as a "current source" on line 21? Also, since current flowing through switch (transistor) MC will have minimal loss due to leakage current within the transistor, the current level at the source of MC is considered equal to the current level at its drain, the load side of current source MC. Therefore, how does the applicant actually equalize the current on both ends of current source MC? Also, if "switch MC is a switched current source" as page 7 of the amendment indicates, what causes it to switch? Only when it is combined with switches MS and/or MT would it be considered a "switched current source" by the examiner. Without at least one of those switches, MC is shown as a constant current source due to the reference voltage applied to its gate. Use of consistent labeling would not "leave the paragraph erroneously descriptive of the invention" as the line lines of page 7 state. It is believed the consistent labeling would actually help to minimize confusion by more clearly identifying what the applicant is actually trying to convey.

3) Lines 4-6 of the amendment's page 7 creates more confusion with respect to what the applicant is attempting to claim. Apparently, all components connected to a current source can be considered the current source's load. Therefore, it is no longer clear what the applicant considers the "substantially continuously" reduced flow to the

load. Using the applicant's own Fig. 5 as an example, is the current and/or charge injection flow from current source 420 to load 430-450 or load 440? Without a clear description of the invention, the claimed limitations are confusing, and meaningful clarifications are required.

4) The applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. In this case, the applicant cites "charge injection, is release when a **switched current source** is switched, not requiring other switch components within the circuit to switch" on page 7, and page 8 states "The current source is equalized with respect to **ITSELF**." From the examiner's viewpoint, the applicant's own current source (e.g. 420 of Fig. 5) does not actually switch, but remains on. Since it is always on, the current flowing into its source will be substantially equal to the current flow out of its drain, which is either routed into 450 or into 430,440. Therefore, the applicant has still not clarified how the claimed pull-down mirror path and transistor switch operate to "equalize a current level produced by said current source." Is the applicant trying to indicate the current flow on both sides of switch 430 is equalized, wherein switch 430 only provides current flow from current source 420 to load 440 when switch 430 conducts? As such, the related objection(s) and/or rejection(s) described by the examiner will not be withdrawn until a satisfactory clarification is received with respect to what is disclosed and what is recited within the claims.

5) The applicant's comments on page 9, lines 4-11 are confusing with respect to the load CL substantially constantly receives "current from the current source switch MC through switch MS." However, on lines 7-8, it is clearly stated that "once switch MS is off and switch MT is on, all current will flow through the pull down mirror path through switch MT". This is obvious to one of ordinary skill in the art. However, without knowing what actually controls the switching times of MT and MS, it is not understood what the applicant actually means by the "load will not receive current during a **very** short period of time during charge injection when current is flowing in the mirror path" as cited on lines 10-11. One of ordinary skill in the art would know that anytime switch MS is open, and MT is closed, the current will flow in the mirror path 450 and not to the load. How long MS remains open, and MT remains closed, depends on their respective control signal (S and IS).

6) The applicant's comment "The mirror path diverts the charge injection to ground when the switch at the current source is initially opened" (lines 18-19 of page 9) appears to support the examiner's interpretation of the claimed limitations with respect to the prior art references. First off, the current source is not opened as the statement implies. Instead, its current is merely diverted from one current path into another. In both of the references cited in the prior art rejections, the current of the current source is diverted to ground when a corresponding transistor switch is initially opened. Even after the initial opening of the transistor switch, the current will continue to be diverted to ground until the transistor switch is closed. For example, current from current source MP1 of Harston is diverted to ground through mirror path MP3 when transistor switch

MP2 is opened. Similarly, current I from current source 11 of Ravon is diverted to ground through mirror path M2,13,14 when transistor switch M1 is opened. Whenever transistor switches MP2 and M1 are conducting (i.e. on or closed), the current will flow to their respective load. Therefore, since charge injection is related to the current flow, it appears the prior art references cited will also have reduced charge injection because of their similar current flow diversion to ground. And whenever transistor switches MP2 and M1 are conducting, their respective load will "substantially continuously" receive the current flow from the current source.

7) Page 10, lines 11-13 cites the applicant has **repeatedly** tried to convey the charge injection is associated with a switched current source (i.e. 420), not switch 430. However, the examiner has **repeatedly** tried to convey to the applicant that current source 420 is not considered a switched current source without at least one of switches 430 or MT (shown in the applicant's Fig. 5). Without either of those switches, current source merely provides current IA continuously to 430-450. It is switch 430 that either allows or prevent current flow load 440.

8) With respect to the Ravon reference, the applicant argues that the load creates the current fluctuations, the examiner rejected the claims as being anticipated, and Ravon does not teach the reduction of charge rejection. The examiner believes that as long as a current flow is switched on and off to a load, there will be charge injection. Without the switching operation of switches MT and MS of the applicant's own Fig. 5, there will be no charge injection once power is provided to current source 420. Since Ravon also shows one current source with its current path being alternately

switched between a load and ground, it is believed that reference corresponds to the applicant's own current source and switches. It is believed the switching can temporarily cause current fluctuations. As far as the claims being anticipated, it is not understood by the examiner what the applicant means. The previous Office Action, mailed on Jun 4, 2002, clearly rejected the claims under 35 U.S.C. 103(a) and used the "obvious" type rejection. Therefore, it appears the applicant is misinterpreting the examiner's rejections and reasoning behind the prior art rejections. The examiner had used the "obvious" type rejections because the Ravon reference did not clearly show or disclose "charge injection." However, as described above, and in previous Office Actions, the circuitry of Ravon is believed to provide a means for reducing charge injection due to its current diversion (e.g. switching), of a current source's current, between a load and ground. As of yet, the applicant has not satisfactorily clarified how the claimed invention reads over the references as interpreted by the examiner. From the applicant's comments, it appears a prior art reference must use the same terminology as the applicant (e.g. "charge injection"). However, the examiner disagrees because various circuits can be the same, or very similar, but use different terminology and/or even leave out obvious type descriptions. To narrow limitations down to lack of a references specific recitation of a term does not allow a reasonable, broad interpretation of the claimed limitations by the examiner. See MPEP 2111.

9) The applicant's arguments with respect to the Harston rejections are similar to those with respect to Ravon reference described above. For example, Hartson fails to disclose, teach, or suggest the reduction of charge rejection. Since these types of

arguments were already described above, it is not necessary to basically repeat them again. Harston shows a current source with its current flow selectively switched to flow to either a load or ground. Therefore, it is believed Harston's circuitry corresponds to the claimed limitations and understanding of the applicant's own invention.

10) Page 15 of the amendment cited that "Switch MC is **NOT** biased by a reference voltage", but by a bias voltage that controls switching. If this is the case, the examiner requests the applicant to clearly point out where in the specification that "V_{BIAS}", shown in Fig. 5 applied to the gate of current source transistor MC (of current source 420) is switched. Without this support, it is believed the current source will continuously provide its current IA, and related switches MS and MT will do the switching.

Due to the confusion related to the claim language, what the applicant indicates is claimed (versus what is actually claimed), how the applicant and examiner interpret the differences between the claimed limitations, and prior art references, and the similarities with the prior art references as described above, the rejections within the previous, and the present, Office Actions are deemed proper.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC

2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund

29 December 2002

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